Patent Application

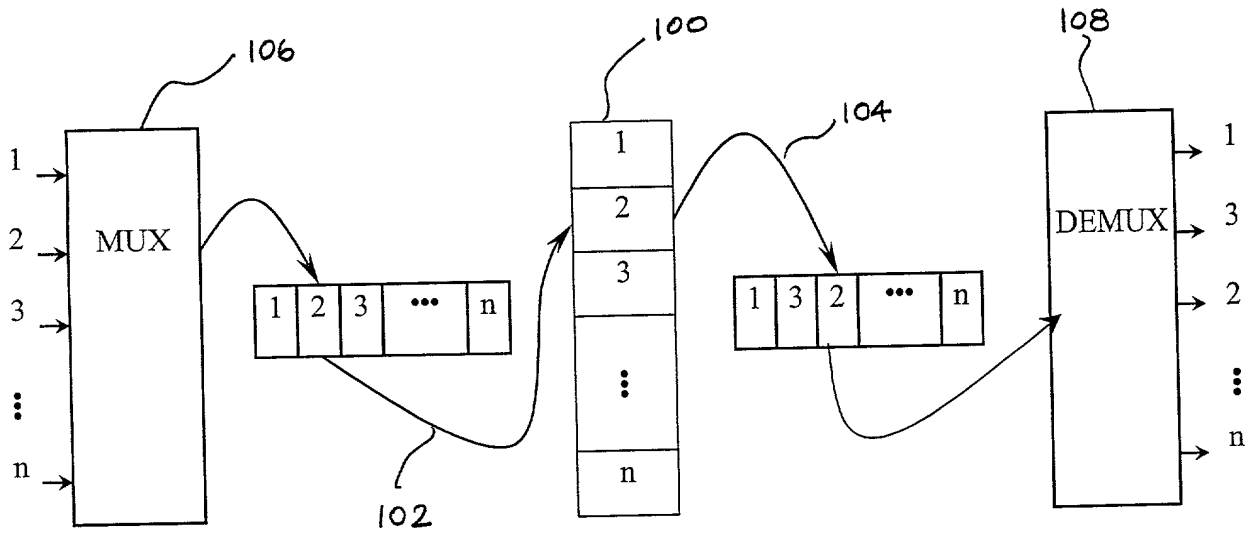


FIG. 1

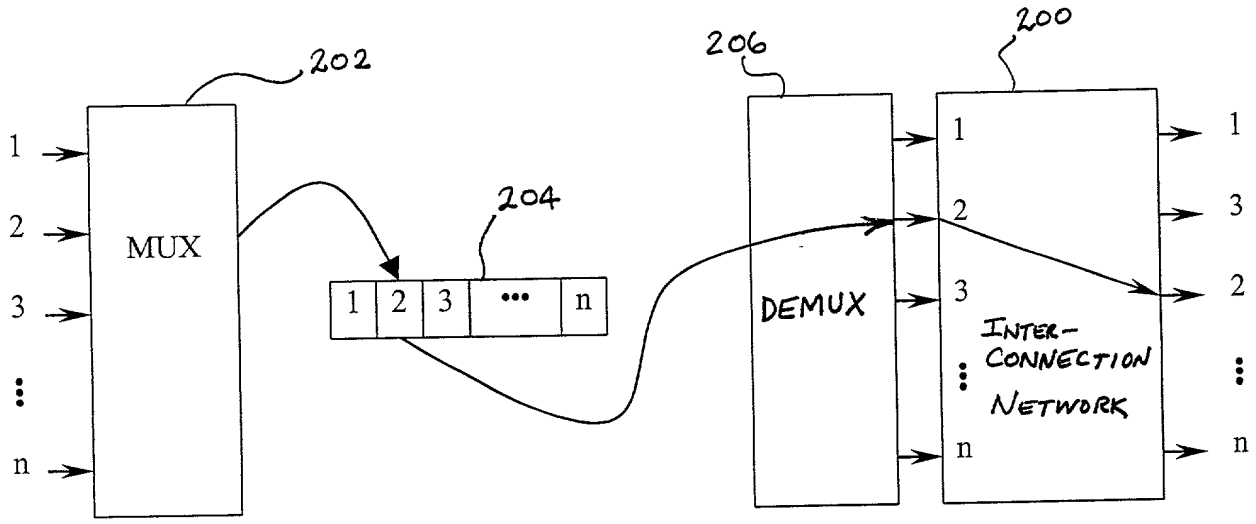

202
206
200
1
2
3
n
MUX
204
1 2 3 ••• n
DEMUX
1
2
3
n
INTER-
CONNECTION
NETWORK
1
3
2
n

FIG. 2

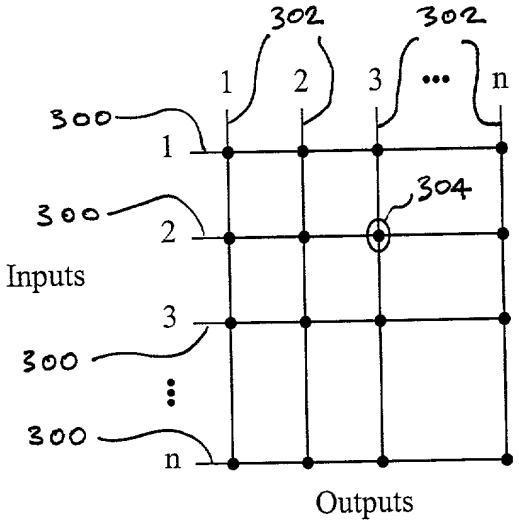

302
302
1 2 3 ••• n
300
1
300
2
304
Inputs
3
300
300
n
Outputs

FIG. 3

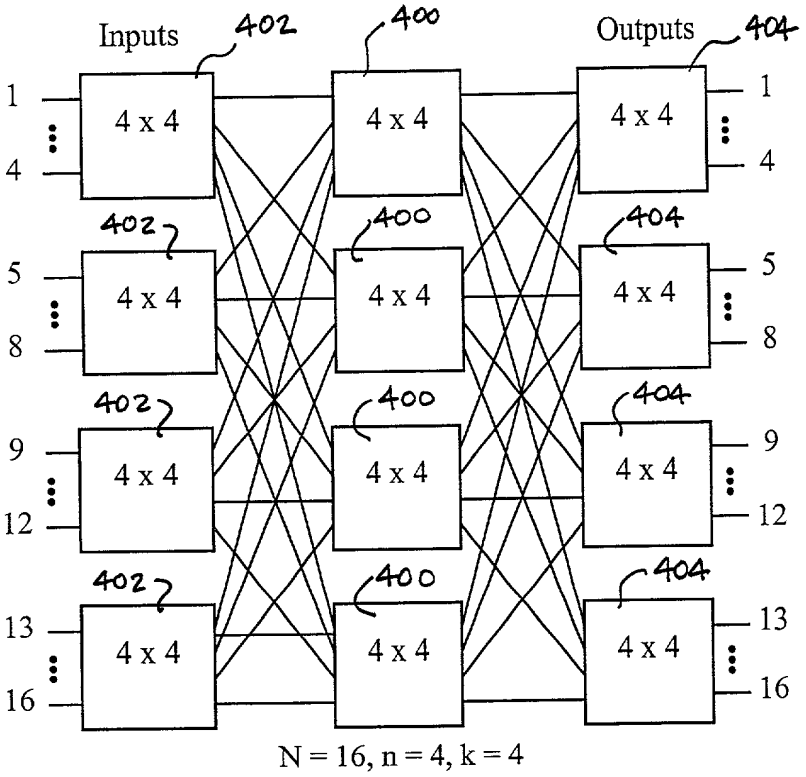

Inputs
Outputs
402
400
404
4 x 4
1
4
5
8
9
12
13
16
N = 16, n = 4, k = 4

FIG. 4

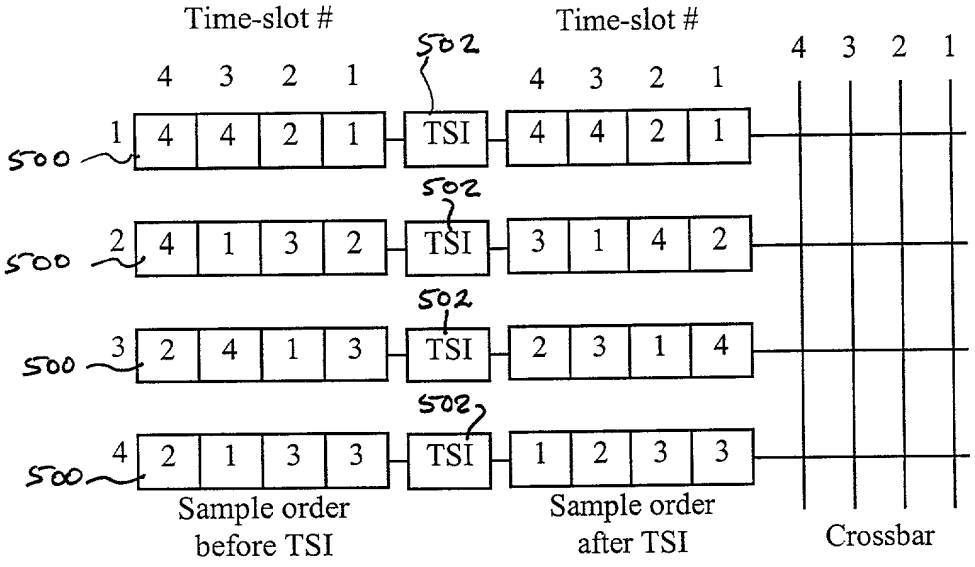

Time-slot #
Time-slot #
4 3 2 1
502
TSI
500
Sample order before TSI
Sample order after TSI
Crossbar

FIG. 5

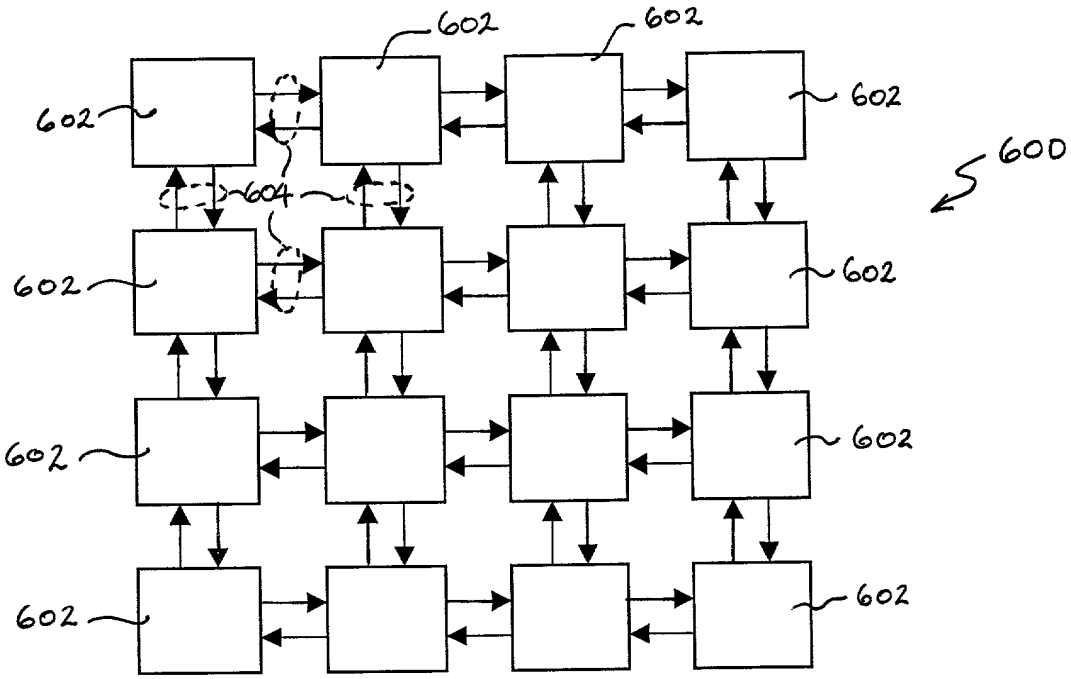
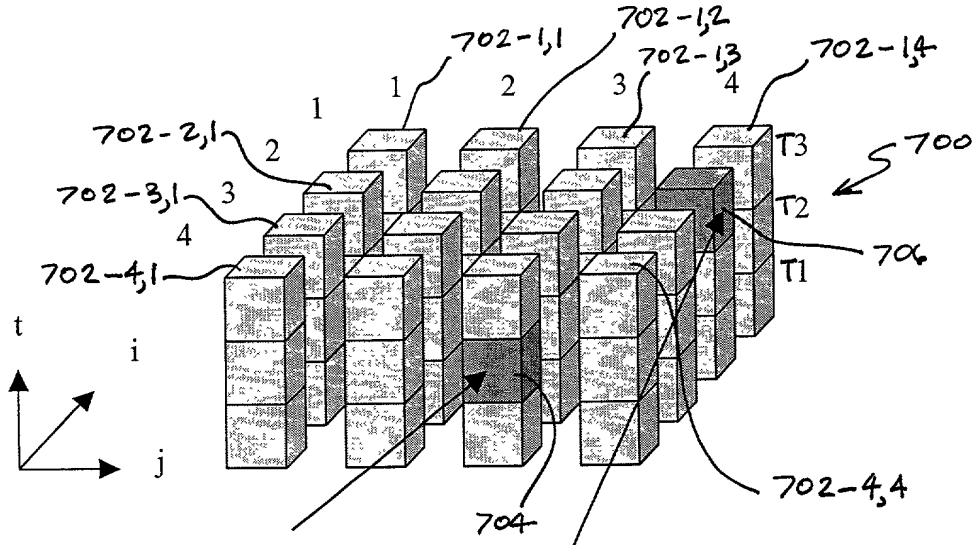


FIG. 6



Source of sample s(i,j,t) = s(4,3,2)

Destination of sample d(i,j,t) = d(2,4,3)

FIG. 7

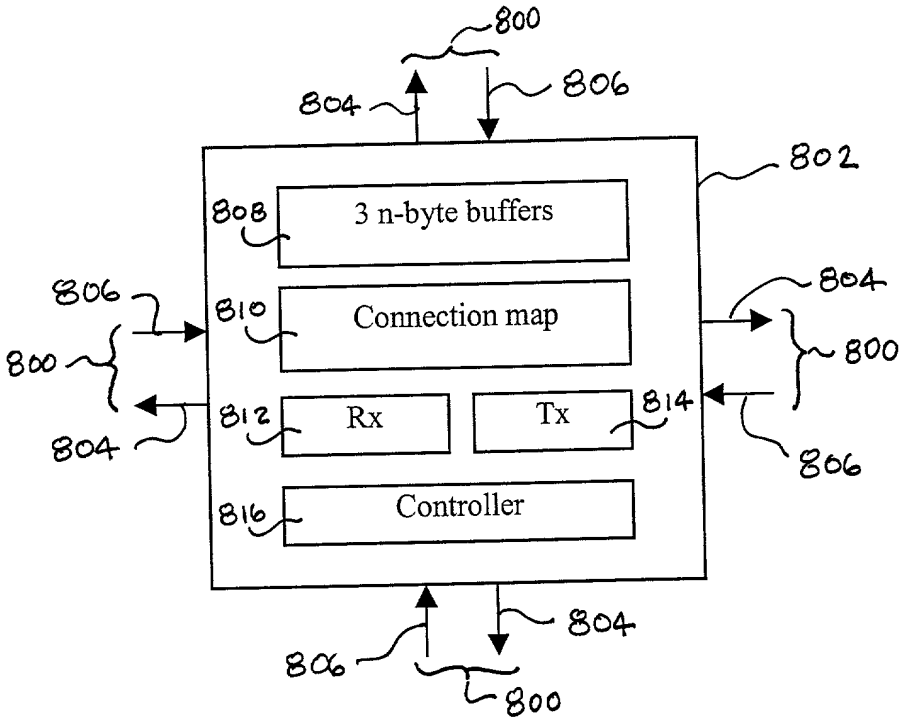

800
804
806
802
808
3 n-byte buffers
806
810
Connection map
804
800
800
812
Rx
Tx
814
804
806
816
Controller
806
804
800

FIG. 8

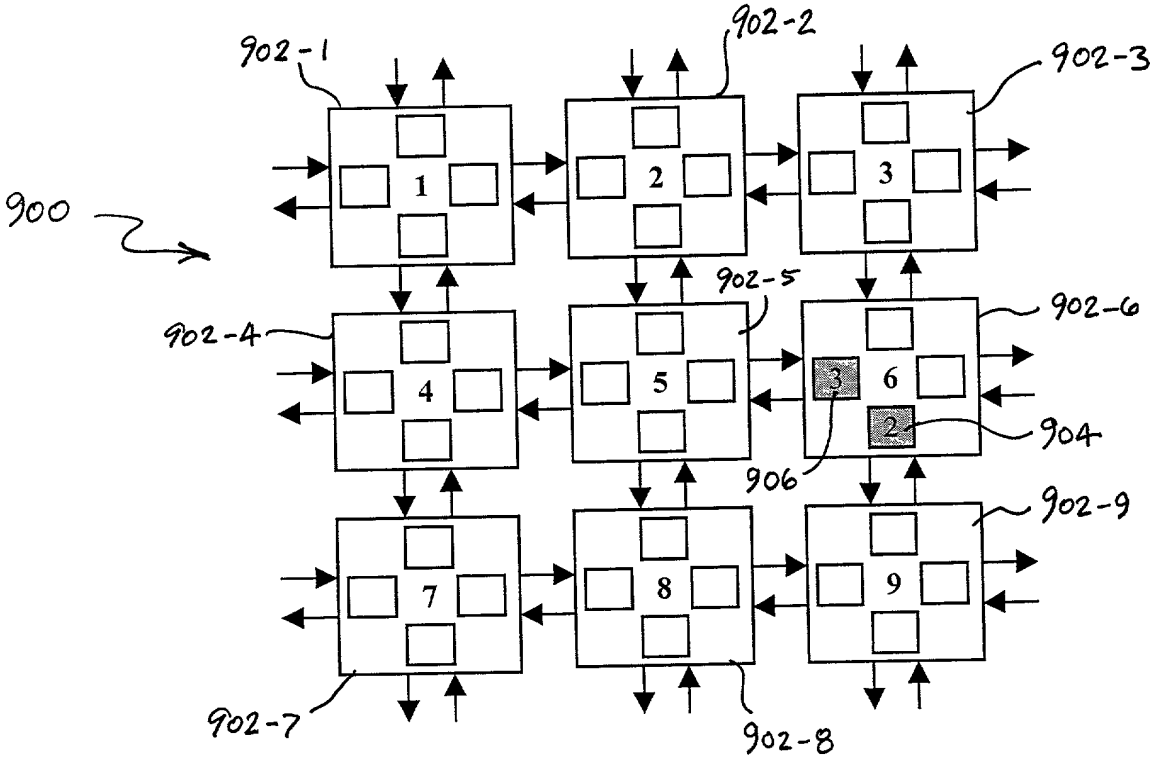

900
902-1
902-2
902-3
1
2
3
902-4
902-5
902-6
4
5
3
6
2
904
906
902-9
7
8
9
902-7
902-8

FIG. 9

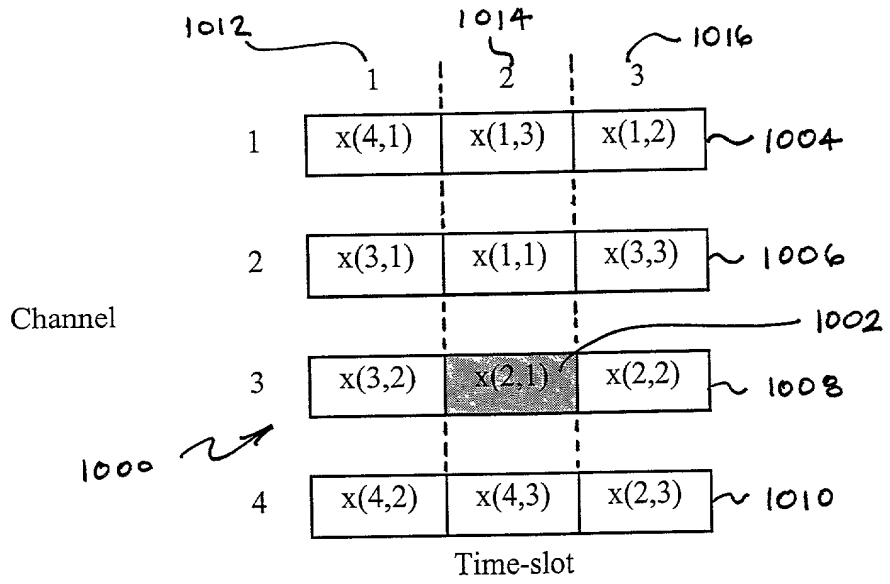


FIG. 10

FOLEY-25250.PCT

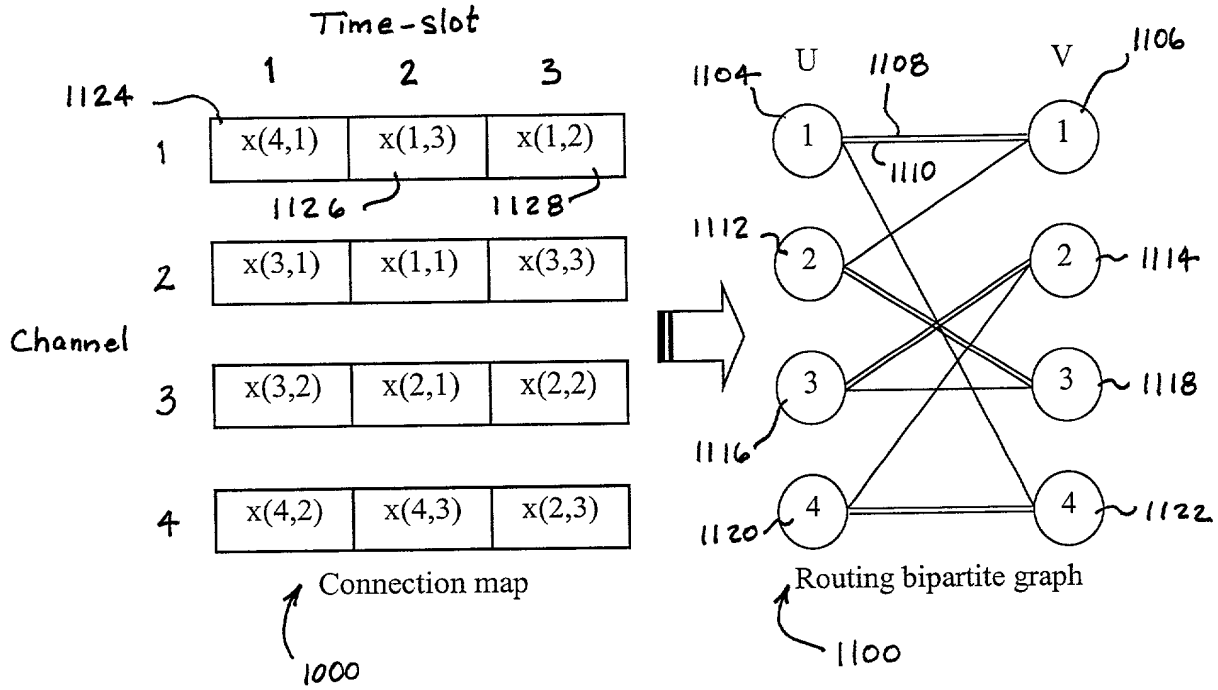
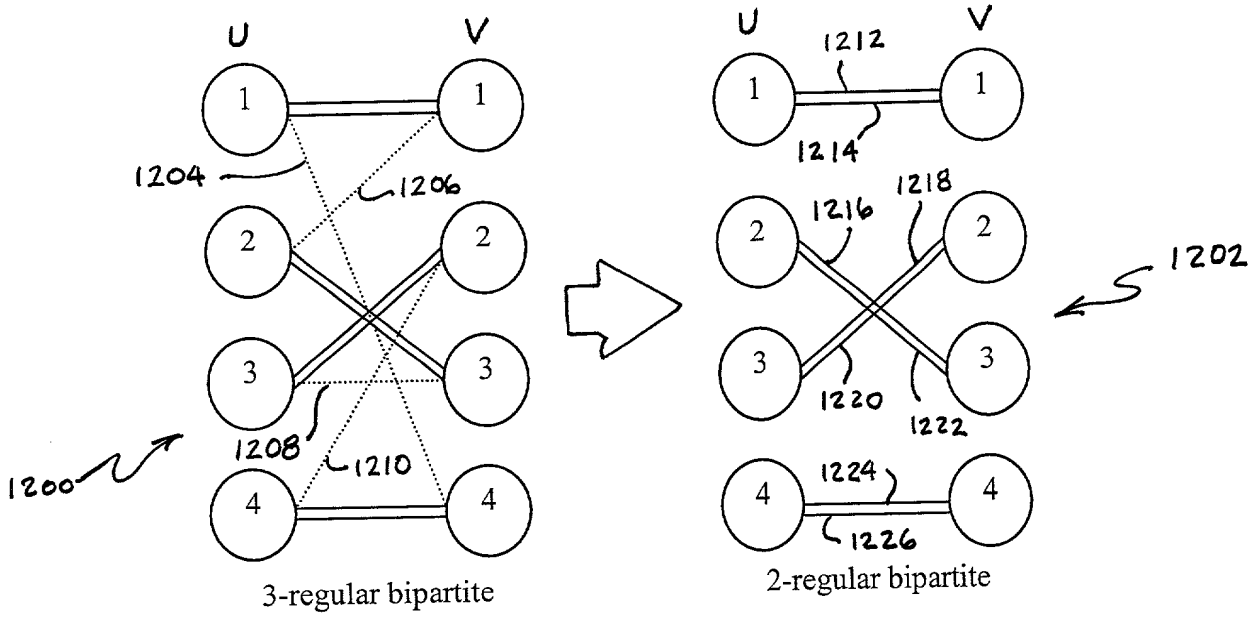


FIG. 11



Maximal matching M_1= ((1,4) (2,1) (3,3) (4,2))

FIG. 12

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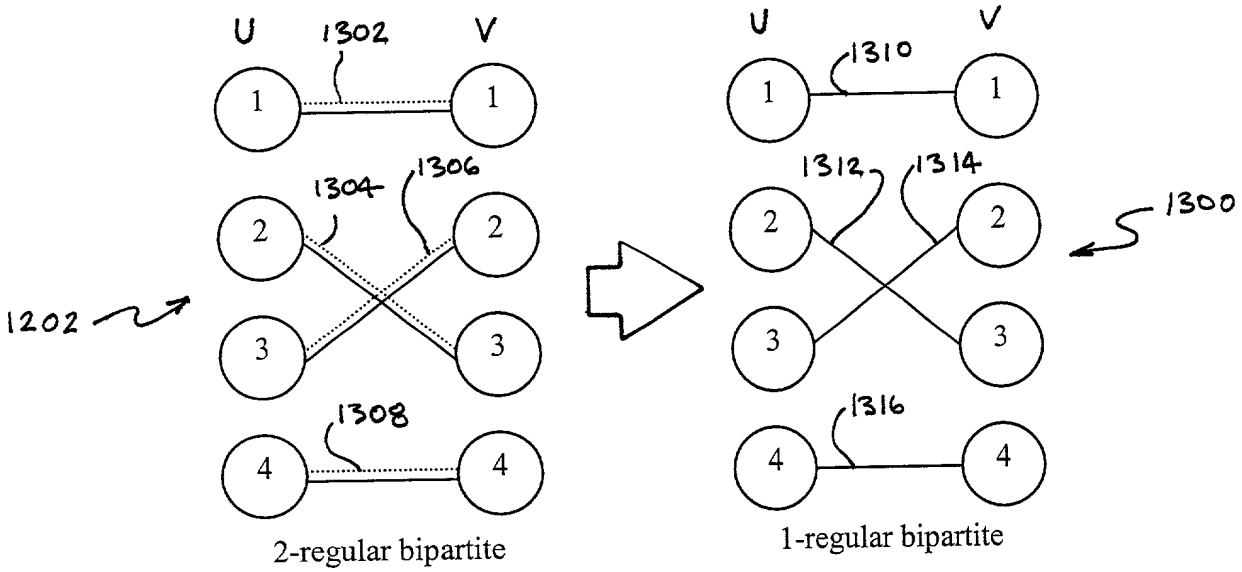


Maximal matching M_2= ((1,1) (2,3) (3,2) (4,4))

FIG. 13

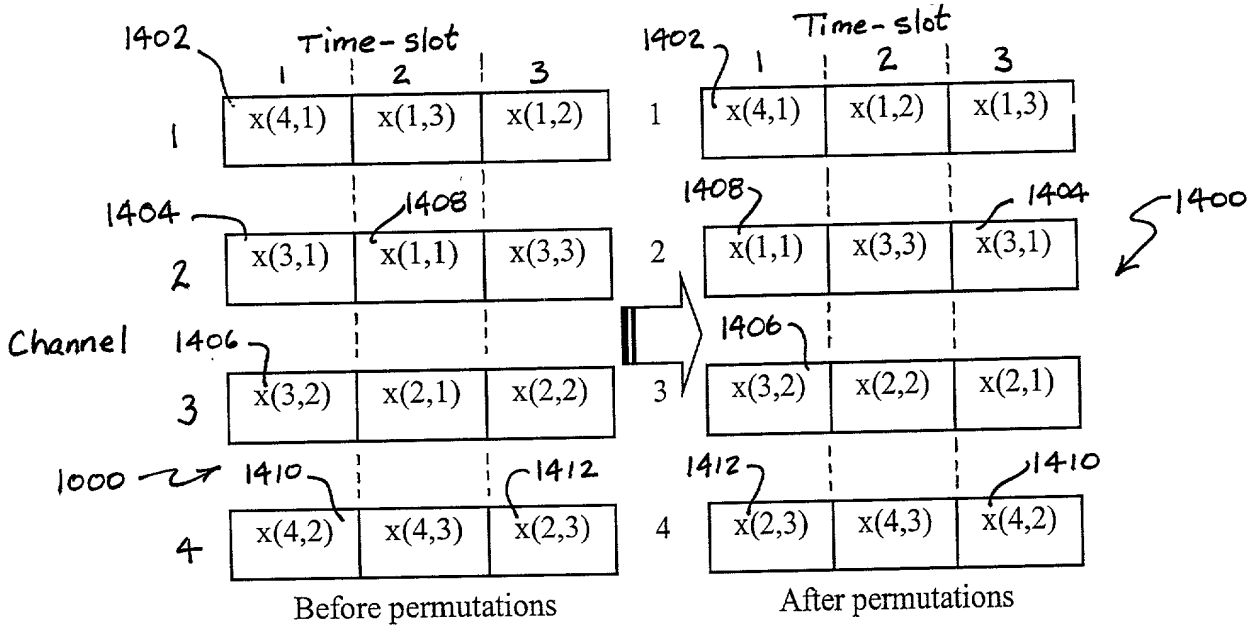
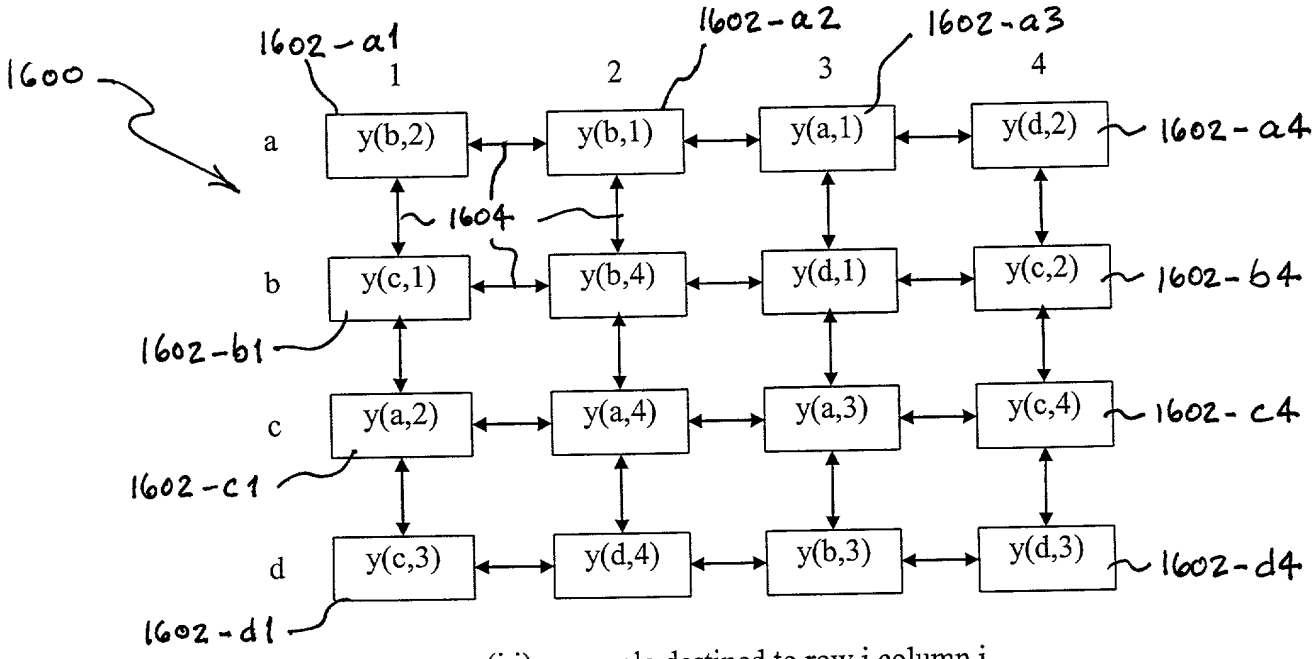


FIG. 14



y(i,j) = sample destined to row i column j

FIG. 16

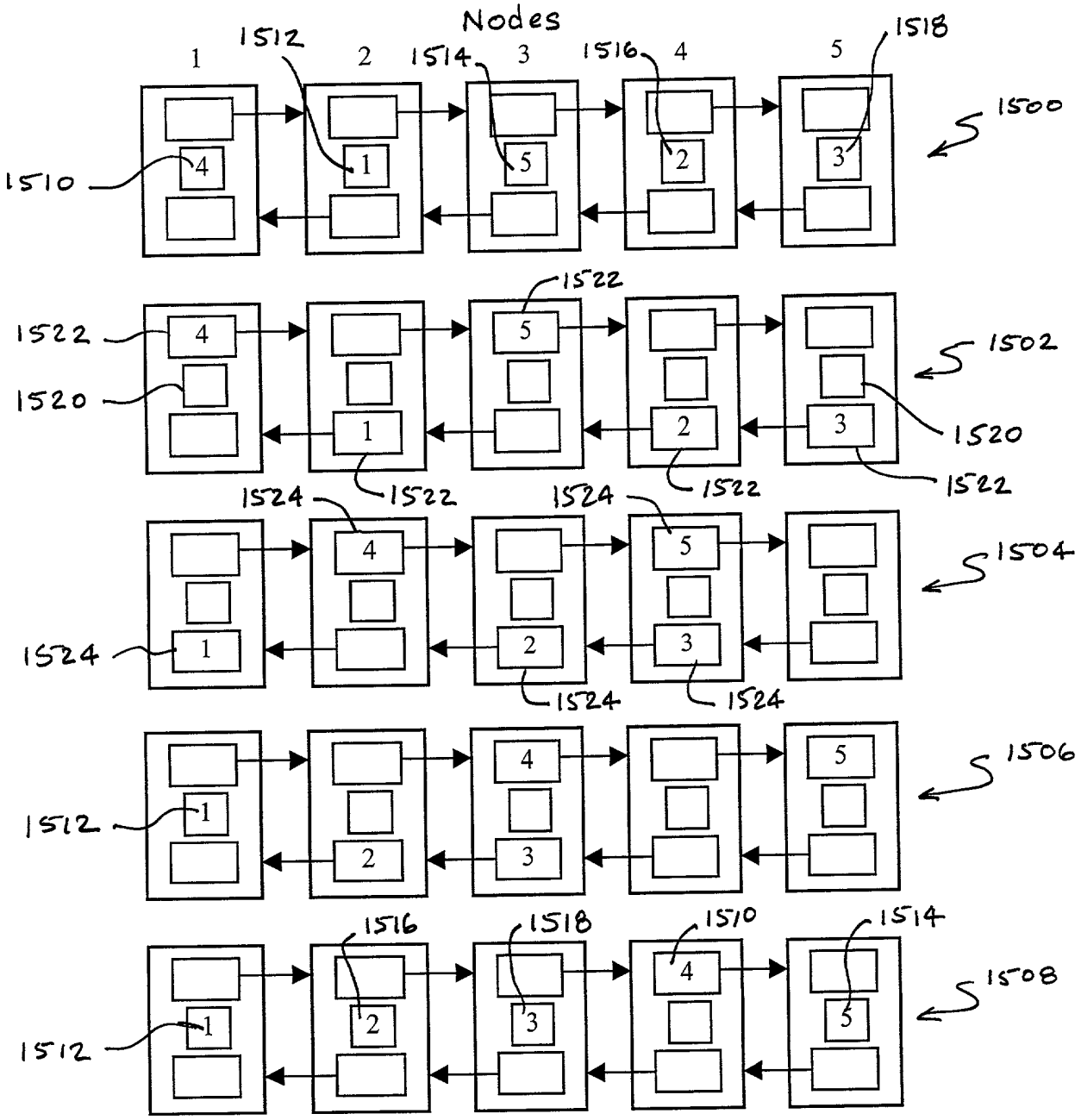

Nodes
1
2
3
4
5
1500
1502
1504
1506
1508
1510
1512
1514
1516
1518
1520
1522
1524

FIG. 15

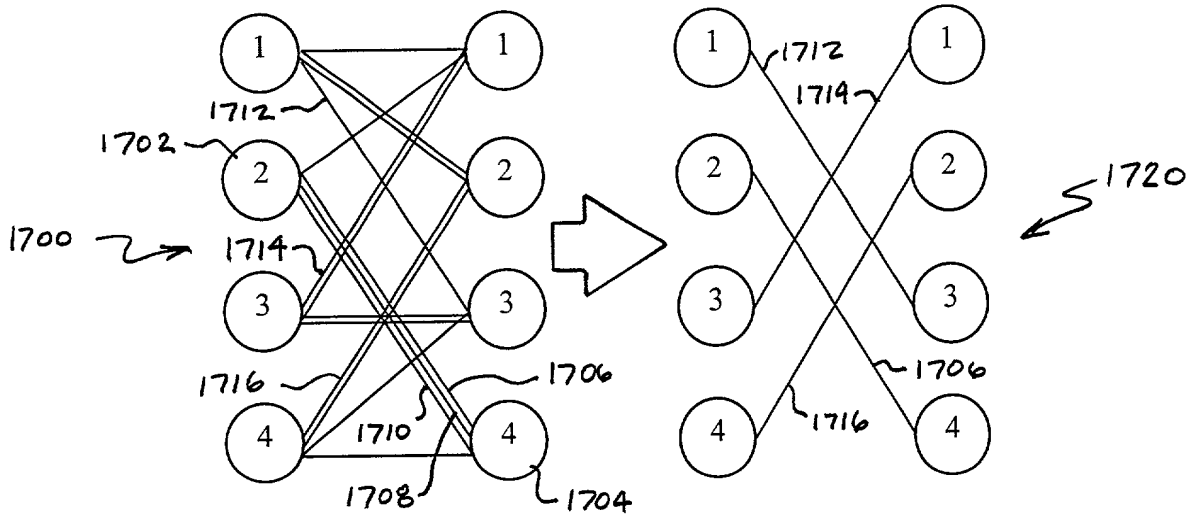


FIG. 17

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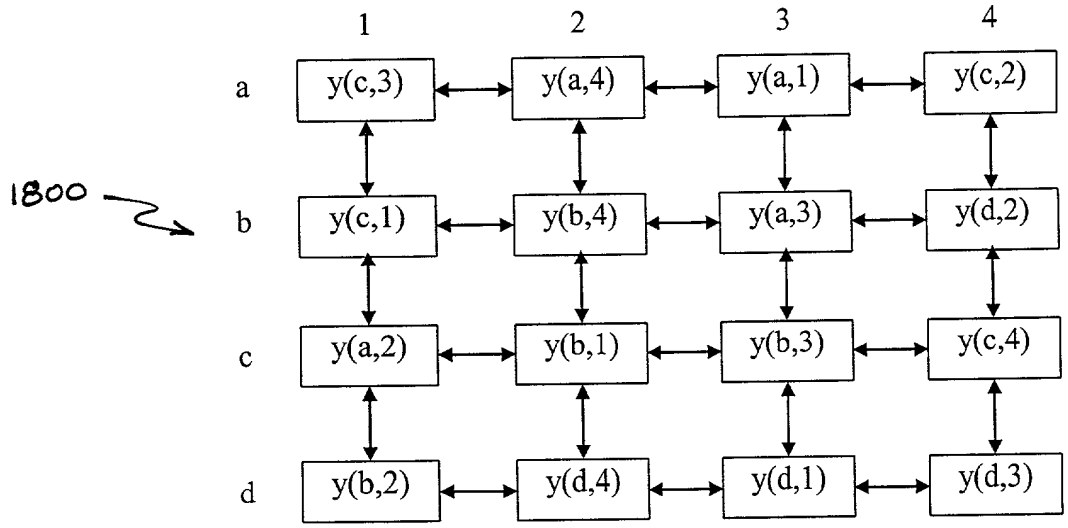
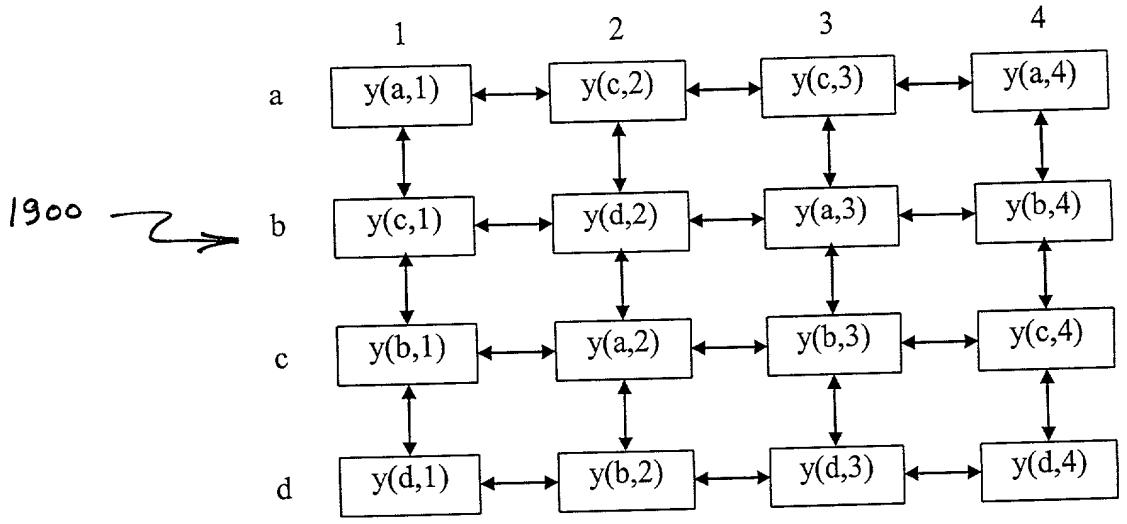


y(i,j) = sample destined to row i column j

FIG. 18



y(i,j) = sample destined to row i column j

FIG. 19

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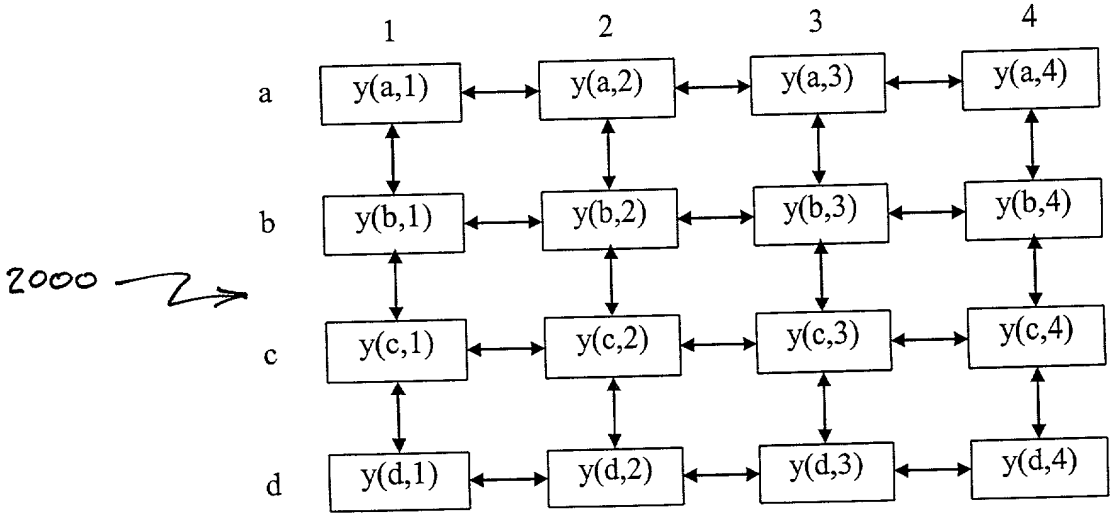

y(i,j) = sample destined to row i column j

FIG. 20

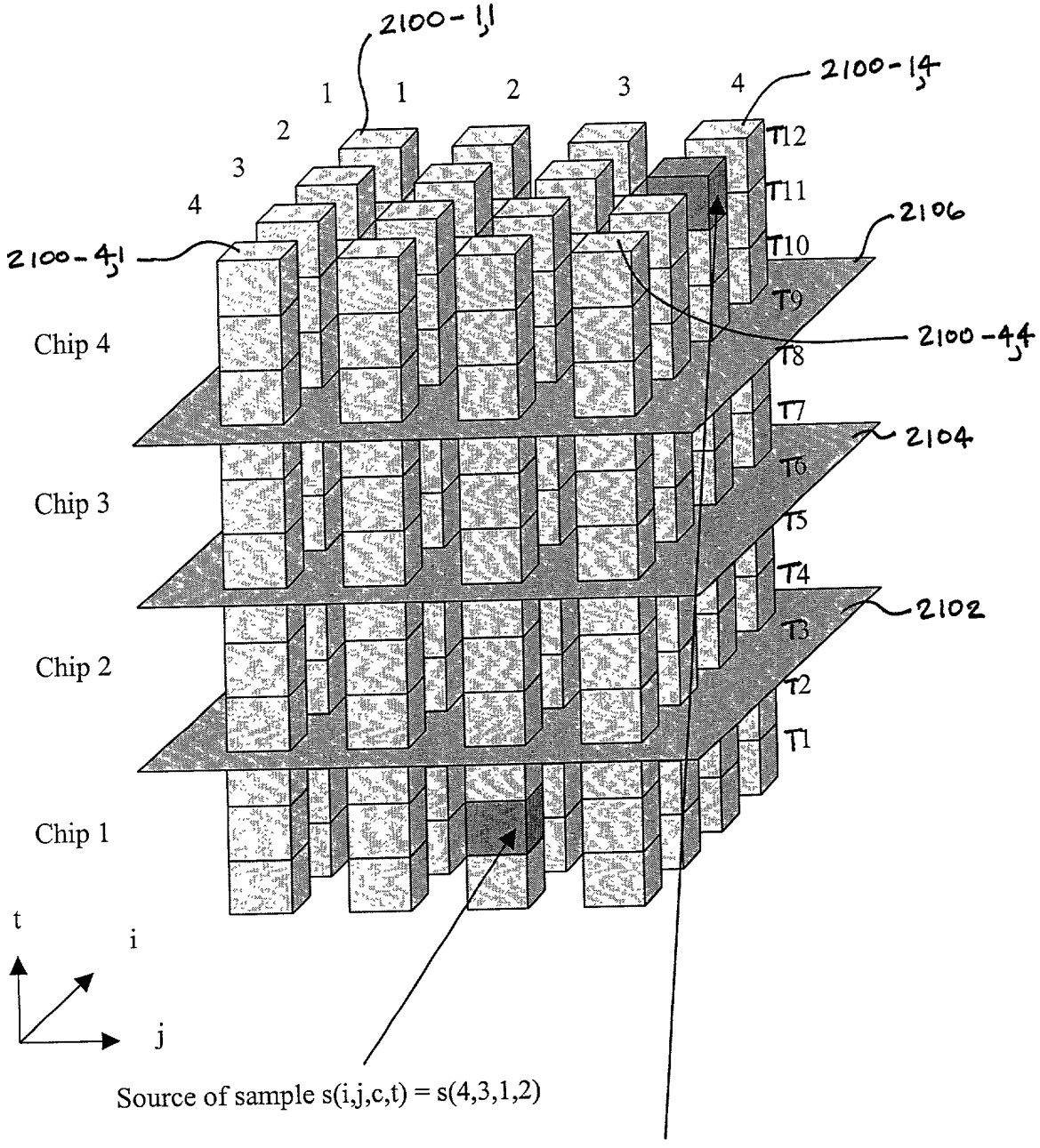
2100-1,1
2100-1,4
2100-4,1
2100-4,4
2106
2104
2102
1
2
3
4
T12
T11
T10
T9
T8
T7
T6
T5
T4
T3
T2
T1
Chip 4
Chip 3
Chip 2
Chip 1
t
i
j
Source of sample s(i,j,c,t) = s(4,3,1,2)
Destination of sample d(i,j,c,t) = d(2,4,4,3)

FIG. 21